

Interference Search

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	0	703/13-15.ccls. and (bidirectional and model and hdl and NMOS).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:42
L3	1	703/13-15.ccls. and (bidirectional and model and wire).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:43
L4	0	703/13-15.ccls. and (NMOS and impedance).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:43
L5	0	703/13-15.ccls. and (NMOS and truth and table).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:44
L6	0	703/13-15.ccls. and (NMOS and (truth adj table)).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:45
L7	1	703/13-15.ccls. and (vHDL and vital).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:46
L8	1	703/13-15.ccls. and (port and control and mechanism).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:46
L9	1	703/13-15.ccls. and (port and delay and annotated).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:46

L10	4	703/13-15.ccls. and (port and enable).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/26 17:47
L11	9	(US-4963863-\$ or US-5202593-\$ or US-5396435-\$ or US-6442738-\$ or US-6496955-\$ or US-6553338-\$ or US-6587999-\$ or US-6751744-\$ or US-6763503-\$).did.	USPAT	OR	OFF	2005/07/26 17:55
L12	5	(US-5455521-\$ or US-5455928-\$ or US-5801549-\$ or US-6480817-\$ or US-6909307-\$).did.	USPAT	OR	OFF	2005/07/26 17:57

Inventor Search

Inventor Name Search Result

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PALM INTRANET

Day : Tuesday
Date : 7/26/2005
Time : 18:36:09

Inventor Name Search Result

Your Search was:

Last Name = GRUPP
First Name = RICHARD

Application#	Patent#	Status	Date Filed	Title	Inventor Name
10906467	Not Issued	030	02/22/2005	MECHANISM TO PROVIDE TEST ACCESS TO THIRD-PARTY MACRO CIRCUITS EMBEDDED IN AN ASIC (APPLICATION-SPECIFIC INTEGRATED CIRCUIT)	GRUPP, RICHARD
10709382	Not Issued	020	04/30/2004	ACCESS METHOD FOR EMBEDDED JTAG TAP CONTROLLER INSTRUCTION REGISTERS	GRUPP, RICHARD
10605747	Not Issued	020	10/23/2003	MULTI-VALUED OR SINGLE STRENGTH SIGNAL DETECTION IN A HARDWARE DESCRIPTION LANGUAGE	GRUPP, RICHARD
09854038	Not Issued	080	05/11/2001	BIDIRECTIONAL WIRE I/O MODEL AND METHOD FOR DEVICE SIMULATION	GRUPP, RICHARD
08232536	Not Issued	150	12/14/1992	METHOD AND APPARATUS FOR POWER MANAGEMENT IN VIDEO SUBSYSTEMS	GRUPP, RICHARD

Inventor Search Completed: No Records to Display.

Search Another: Inventor

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PALM INTRANET

Day : Tuesday
Date: 7/26/2005
Time: 18:36:48

Inventor Name Search Result

Your Search was:

Last Name = TSYRKINA
First Name = YELENA

Application#	Patent#	Status	Date Filed	Title	Inventor Name
02854038	Not Issued	080	05/11/2001	BIDIRECTIONAL WIRE I/O MODEL AND METHOD FOR DEVICE SIMULATION	TSYRKINA, YELENA M.

Inventor Search Completed: No Records to Display.

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S22 4	307	703/15.cds.	USPAT	OR	OFF	2005/07/26 17:38
S22 3	167	703/16.cds.	USPAT	OR	OFF	2005/07/26 17:31
S22 2	319	S221 and model	USPAT	OR	OFF	2005/07/26 17:24
S22 1	551	S220 and (bidirectional (bi adj directional))	USPAT	OR	OFF	2005/07/26 17:21
S22 0	5306	703/1-28.cds.	USPAT	OR	OFF	2005/07/26 17:20
S21 8	277	703/21.cds.	USPAT	OR	OFF	2005/07/26 17:19
S21 7	233	703/25.cds.	USPAT	OR	OFF	2005/07/26 17:18
S21 6	157	703/17.cds.	USPAT	OR	OFF	2005/07/26 17:14
S21 3	0	timing with simulat\$ with input with port with delay	USPAT; USOCR; EPO; JPO; DERIVENT; IBM_TDB	OR	OFF	2005/07/26 13:13
S21 2	0	annotate with timing with simulat\$ with input with port with delay	USPAT; USOCR; EPO; JPO; DERIVENT; IBM_TDB	OR	OFF	2005/07/26 13:13
S21 0	1506	annotate timing with simulat\$ with input with port with delay	USPAT; USOCR; EPO; JPO; DERIVENT; IBM_TDB	OR	OFF	2005/07/26 13:13
S21 1	1329	S210	USPAT	OR	OFF	2005/07/26 13:11
S20 9	8	S208 and (wire and delay)	USPAT	OR	OFF	2005/07/26 13:11
S20 8	233	703/25.cds.	USPAT	OR	OFF	2005/07/26 12:56
S17 5	233	703/25.cds.	USPAT	OR	OFF	2005/07/26 12:56
S20 7	80	(bus adj) repeater) and (model\$5 simulat\$6)	USPAT	OR	OFF	2005/07/25 19:10
S11 3	30	("4161786" "4604689" "4768188" "4837788" "4974153" "5036473").PN. OR ("5202593").URPN.	US-PCRPUB; USPAT; USOCR	OR	OFF	2005/07/25 19:01

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S20 3	0	S202 near wire near load	USPAT	OR	OFF	2005/07/25 18:59
S20 2	52	verilog near model	USPAT	OR	OFF	2005/07/25 18:59
S20 1	1	"09/854038"	US-PCRPUB	OR	OFF	2005/07/25 18:34
S20 0	31	("4161786" "4604689" "4768188" "4837788" "4974153" "5036473").PN. OR ("5202593").URPN.	US-PCRPUB; USPAT; USOCR	OR	OFF	2005/07/25 15:47
S19 9	1	"5202593".pn.	US-PCRPUB; USPAT; USOCR	OR	OFF	2005/07/25 15:47
S19 8	43	verilog same media same disk\$	USPAT	OR	OFF	2005/07/25 15:47
S19 7	201	S195 and disks	USPAT	OR	OFF	2005/07/25 15:47
S19 6	1	S195 and CDROM	USPAT	OR	OFF	2005/07/25 15:47
S19 5	584	verilog and media	USPAT	OR	OFF	2005/07/25 15:47
S19 4	185	verilog and VHDL and (timing with delay)	USPAT	OR	OFF	2005/07/25 15:47
S19 3	160	verilog and HDL and (timing with delay)	USPAT	OR	OFF	2005/07/25 15:47
S19 2	76	input adj2 port adj delay	USPAT	OR	OFF	2005/07/25 15:47
S19 1	185	input adj2 port adj2 delay	USPAT	OR	OFF	2005/07/25 15:47
S19 0	197	input and port adj delay	USPAT	OR	OFF	2005/07/25 15:47
S18 9	51	timing adj report	USPAT	OR	OFF	2005/07/25 15:47
S18 8	40	S187 and verilog	USPAT	OR	OFF	2005/07/25 15:47
S18 7	1504	annotate timing with simulat\$ with input with port with delay	USPAT; USOCR; EPO; JPO; DERIVENT; IBM_TDB	OR	OFF	2005/07/25 15:47
S18 6	2	S185 and NMOS	USPAT	OR	OFF	2005/07/25 15:47
S18 5	75	S184 same (simulat\$ or emulat\$ or model\$ or process\$ or execut\$)	USPAT	OR	OFF	2005/07/25 15:47
S18 4	267	timing with delay with port	USPAT	OR	OFF	2005/07/25 15:47

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Updated End E. Alex Rendell

S18 3	29339	timing with delay	USPAT	OR	OFF	2005/07/25 15:47
S18 2	3	timing with propagation with delay	USPAT	OR	OFF	2005/07/25 15:47
S18 1	22	S178 with signal	USPAT	OR	OFF	2005/07/25 15:47
S18 0	0	S178 with signal with integrity	USPAT	OR	OFF	2005/07/25 15:47
S17 9	1	S178 with directional	USPAT	OR	OFF	2005/07/25 15:47
S17 8	369	virtual with port with connection	USPAT	OR	OFF	2005/07/25 15:47
S17 7	2	NMOS with verilog	USPAT	OR	OFF	2005/07/25 15:47
S17 6	8	S175 and verilog	USPAT	OR	OFF	2005/07/25 15:47
S17 4	8	crosspoint with NMOS	USPAT	OR	OFF	2005/07/25 15:47
S17 3	0	HDL same (channel with bi-directional)	US-PCPUB; USPAT; USOCR; EPO; JPO; DERVENT; IBM_TDB	OR	OFF	2005/07/25 15:47
S17 2	141	HDL same channel	US-PCPUB; USPAT; USOCR; EPO; JPO; DERVENT; IBM_TDB	OR	OFF	2005/07/25 15:47
S17 1	22	S170 and (detection same change)	US-PCPUB; USPAT; USOCR; EPO; JPO; DERVENT; IBM_TDB	OR	OFF	2005/07/25 15:47
S17 0	526	HDL and Channel and (bus or path) and port	US-PCPUB; USPAT; USOCR; EPO; JPO; DERVENT; IBM_TDB	OR	OFF	2005/07/25 15:47
S16 9	47	HDL and (Bus adl functional adl Model)	US-PCPUB; USPAT; DERVENT	OR	OFF	2005/07/25 15:47
S16 8	36	S167 and port and matching	US-PCPUB; USPAT; DERVENT	OR	OFF	2005/07/25 15:47

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S16 7	240	HDL same path	US-PCPUB; USPAT; DERVENT	OR	OFF	2005/07/25 15:47
S16 6	10527	HDL	US-PCPUB; USPAT; DERVENT	OR	OFF	2005/07/25 15:47
S16 5	11	S164 and path and (change same detection)	US-PCPUB; USPAT; DERVENT	OR	OFF	2005/07/25 15:47
S16 4	283	HDL same port	US-PCPUB; USPAT; DERVENT	OR	OFF	2005/07/25 15:47
S16 3	3	S162 and (change same detection)	US-PCPUB; USPAT; DERVENT	OR	OFF	2005/07/25 15:47
S16 2	82	S161 and HDL	US-PCPUB; USPAT; DERVENT	OR	OFF	2005/07/25 15:47
S16 1	7980	port same programming	US-PCPUB; USPAT; DERVENT	OR	OFF	2005/07/25 15:47
S16 0	1	1996KR-0018252	US-PCPUB; USPAT; DERVENT	OR	OFF	2005/07/25 15:47
S15 9	46	(bi-directional with buffer).ti.	US-PCPUB; USPAT; DERVENT	OR	OFF	2005/07/25 15:47
S15 8	1	1997GB-0024259	US-PCPUB; USPAT; DERVENT	OR	OFF	2005/07/25 15:47
S15 7	1	"20040162711"	US-PCPUB; USPAT	OR	OFF	2005/07/25 15:47
S15 6	0	S155 near wire near load	USPAT	OR	OFF	2005/07/25 15:47
S15 5	52	verilog near model	USPAT	OR	OFF	2005/07/25 15:47
S15 4	21	("4488354" "4683384" "4744084" "4791357" "4821173" "4942317" "4978633" "4980889" "5105373" "5166937" "5300835" "5317698" "5406147" "5426591" "5426739" "5428750" "5452229" "5479123" "5481484" "5535223" "5572437").PN.	US-PCPUB; USPAT; USOCR	OR	OFF	2005/07/25 15:47
S15 3	3	("6480817").URNP.	USPAT	OR	OFF	2005/07/25 15:47
S15 2	20	model same (10 near pad)	USPAT	OR	OFF	2005/07/25 15:47

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S15	4	S149 same load	USPAT	OR	OFF	2005/07/25 15:47
S15	0	S149 same verilog	USPAT	OR	OFF	2005/07/25 15:47
S14	69	S148 with model	USPAT	OR	OFF	2005/07/25 15:47
S14	1440	simulate\$ with wire	USPAT	OR	OFF	2005/07/25 15:47
S14	3311	simulate\$ same wire	USPAT	OR	OFF	2005/07/25 15:47
S14	1	"6594598".pn.	USPAT	OR	OFF	2005/07/25 15:47
S14	1	"6496955".pn.	USPAT	OR	OFF	2005/07/25 15:47
S14	1	"5999734".pn.	USPAT	OR	OFF	2005/07/25 15:47
S14	52	half adj duplex adj modem	USPAT	OR	OFF	2005/07/25 15:47
S14	1	NN9012277	DERWENT; IBM_TDB	OR	OFF	2005/07/25 15:47
S14	11	S140 with path	USPAT	OR	OFF	2005/07/25 15:47
S14	355	(interconnect adj2 model\$)	USPAT	OR	OFF	2005/07/25 15:47
S13	4	(interconnect adj2 model\$) same load same delay	USPAT	OR	OFF	2005/07/25 15:47
S13	76	verilog and tran	USPAT	OR	OFF	2005/07/25 15:47
S13	1	annotate with path with delay	USPAT	OR	OFF	2005/07/25 15:47
S13	33	wire adj load adj model	USPAT	OR	OFF	2005/07/25 15:47
S13	12	S134 same simulate\$	USPAT	OR	OFF	2005/07/25 15:47
S13	148	wire adj model	USPAT	OR	OFF	2005/07/25 15:47
S13	1	((wire or path or line) adj (load or delay) adj (simulate\$ or emulate\$ or model)) same verilog	USPAT	OR	OFF	2005/07/25 15:47
S13	9	("5610833" "5629860" "5694344" "5706206" "6175947" "6189131" "6243653" "6291254" "6381730").pn.	US-PCPUB; USPAT; USOCR	OR	OFF	2005/07/25 15:47
S13	0	(US-6763503-\$).did.	USPAT	OR	OFF	2005/07/25 15:47

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S13	5	(model with wire).it.	USPAT	OR	OFF	2005/07/25 15:47
S12	0	characterize with wire with delay	USPAT	OR	OFF	2005/07/25 15:47
S12	64	model with wire with delay	USPAT	OR	OFF	2005/07/25 15:47
S12	27	timing with annotation with wire	USPAT	OR	OFF	2005/07/25 15:47
S12	34	S125 with timing	USPAT	OR	OFF	2005/07/25 15:47
S12	3100	wire with model	USPAT	OR	OFF	2005/07/25 15:47
S12	0	wire with timing with I/O with model	USPAT	OR	OFF	2005/07/25 15:47
S12	2	(US-5428750-\$ or US-5300835-\$).did.	USPAT	OR	OFF	2005/07/25 15:47
S12	21	("4488354" "4683394" "4744084" "4791357" "4821173" "4942317" "4978633" "4980889" "5105373" "5166937" "5300835" "5317698" "5406147" "5426591" "5426739" "5428750" "5452229" "5479123" "5481484" "5535223" "5572437").pn.	US-PCPUB; USPAT; USOCR	OR	OFF	2005/07/25 15:47
S12	1	("6480817").pn.	USPAT	OR	OFF	2005/07/25 15:47
S12	109	S117 same (port or node) same (path or loop or mesh)	USPAT	OR	OFF	2005/07/25 15:47
S11	5	S117 same (Verilog and VHDL)	USPAT	OR	OFF	2005/07/25 15:47
S11	109	S117 same (port or node) same (path or loop or mesh)	USPAT	OR	OFF	2005/07/25 15:47
S11	15280	S115 with S116	USPAT	OR	OFF	2005/07/25 15:47
S11	2356320	(bidirection\$ or (two adj2 way) or inout or duplex)) near\$3 (wire or line)	USPAT	OR	OFF	2005/07/25 15:47
S11	184343	(simulate\$ or emulate\$)	USPAT	OR	OFF	2005/07/25 15:47
S11	79	(bus adj repeater) and (model\$5 simulate\$6)	USPAT	OR	OFF	2005/05/03 13:58
S11	38	verilog same media same disk\$	USPAT	OR	OFF	2005/05/03 13:57
S90	3	timing with propagation with delay	USPAT	OR	OFF	2005/05/03 13:56

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S111	1	"S20293".ipn.	US-PGRUB; USPAT; USOCR;	OR	OFF	2005/05/03 11:21
S112	179	S108 and disks	USPAT	OR	OFF	2004/12/30 16:14
S110	1	S108 and CDROM	USPAT	OR	OFF	2004/12/30 16:14
S108	501	verilog and media	USPAT	OR	OFF	2004/12/30 16:12
S107	169	verilog and VHDL and (timing with delay)	USPAT	OR	OFF	2004/12/29 14:49
S106	145	verilog and HDL and (timing with delay)	USPAT	OR	OFF	2004/12/29 14:49
S96	1402	annotate timing with simulat\$ with input with port with delay	USPAT; USOCR; EPO; JPO; DERVENT; IBM_TDB	OR	OFF	2004/12/29 14:32
S104	76	input adj2 port adj delay	USPAT	OR	OFF	2004/12/29 14:31
S103	180	input adj2 port adj2 delay	USPAT	OR	OFF	2004/12/29 14:29
S102	195	input and port adj delay	USPAT	OR	OFF	2004/12/29 14:26
S101	49	timing adj report	USPAT	OR	OFF	2004/12/29 14:25
S100	37	S96 and verilog	USPAT	OR	OFF	2004/12/29 14:01
S94	2	S93 and NMOS	USPAT	OR	OFF	2004/12/29 13:53
S93	71	S92 same (simulat\$ or emulat\$ or model\$ or process\$ or execut\$)	USPAT	OR	OFF	2004/12/29 13:53
S92	258	timing with delay with port	USPAT	OR	OFF	2004/12/29 13:48
S91	28458	timing with delay	USPAT	OR	OFF	2004/12/29 13:46
S87	1	S86 with directional	USPAT	OR	OFF	2004/12/29 13:42
S89	21	S86 with signal	USPAT	OR	OFF	2004/12/29 10:10
S88	0	S86 with signal with integrity	USPAT	OR	OFF	2004/12/29 10:09
S86	362	virtual with port with connection	USPAT	OR	OFF	2004/12/29 10:06
S85	2	NMOS with verilog	USPAT	OR	OFF	2004/12/29 10:06
S78	8	crosspoint with NMOS	USPAT	OR	OFF	2004/12/28 16:03
S83	7	S81 and verilog	USPAT	OR	OFF	2004/12/28 15:48
S81	227	703/25.cds.	USPAT	OR	OFF	2004/12/28 15:48

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S77	0	HDL same (channel with bi-directional)	US-PGRUB; USPAT; USOCR; EPO; JPO; DERVENT; IBM_TDB	OR	OFF	2004/12/27 16:04
S76	121	HDL same channel	US-PGRUB; USPAT; USOCR; EPO; JPO; DERVENT; IBM_TDB	OR	OFF	2004/12/27 15:43
S75	21	S74 and (detection same change)	US-PGRUB; USPAT; USOCR; EPO; JPO; DERVENT; IBM_TDB	OR	OFF	2004/12/27 15:41
S74	446	HDL and Channel and (bus or path) and port	US-PGRUB; USPAT; USOCR; EPO; JPO; DERVENT; IBM_TDB	OR	OFF	2004/12/27 15:38
S63	45	(bi-directional with buffer) it.	US-PGRUB; USPAT; USOCR; EPO; JPO; DERVENT; IBM_TDB	OR	OFF	2004/12/27 15:36
S73	43	HDL and (Bus adj functional adj Model)	US-PGRUB; USPAT; USOCR; EPO; JPO; DERVENT; IBM_TDB	OR	OFF	2004/12/27 15:27
S72	34	S71 and port and matching	US-PGRUB; USPAT; USOCR; EPO; JPO; DERVENT; IBM_TDB	OR	OFF	2004/12/27 15:27
S71	216	HDL same path	US-PGRUB; USPAT; USOCR; EPO; JPO; DERVENT; IBM_TDB	OR	OFF	2004/12/27 15:26
S70	9226	HDL	US-PGRUB; USPAT; USOCR; EPO; JPO; DERVENT; IBM_TDB	OR	OFF	2004/12/27 15:25
S69	8	S68 and path and (change same detection)	US-PGRUB; USPAT; USOCR; EPO; JPO; DERVENT; IBM_TDB	OR	OFF	2004/12/27 15:25
S68	248	HDL same port	US-PGRUB; USPAT; USOCR; EPO; JPO; DERVENT; IBM_TDB	OR	OFF	2004/12/27 15:22
S67	2	S66 and (change same detection)	US-PGRUB; USPAT; USOCR; EPO; JPO; DERVENT; IBM_TDB	OR	OFF	2004/12/27 15:22
S66	72	S65 and HDL	US-PGRUB; USPAT; USOCR; EPO; JPO; DERVENT; IBM_TDB	OR	OFF	2004/12/27 15:20

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S65	7229	port same programming	US-PCPUB; USPAT; DERVENT	OR	OFF	2004/12/27 15:20
S64	1	1996KR-0018252	DERVENT	OR	OFF	2004/12/27 14:39
S61	1	1997GB-0024259	US-PCPUB; USPAT; DERVENT	OR	OFF	2004/12/27 14:37
S60	1	"20040162711"	US-PCPUB; USPAT	OR	OFF	2004/12/27 14:05
S54	0	S53 near wire near load	USPAT	OR	OFF	2004/12/27 11:15
S53	49	verilog near model	USPAT	OR	OFF	2004/12/27 11:14
S50	20	model same (I/O near pad)	USPAT	OR	OFF	2004/12/27 11:13
S52	21	("4483354" "4683384" "4744084" "4791357" "4821173" "4942317" "4978633" "4980889" "5105373" "5166937" "5300835" "5317698" "5406147" "5426591" "5426739" "5428750" "5452229" "5479123" "5481484" "5535223" "5572437").PN.	US-PCPUB; USPAT; USOCR	OR	OFF	2004/12/27 11:07
S51	2	("6480817").URPN.	USPAT	OR	OFF	2004/12/27 11:07
S47	66	S46 with model	USPAT	OR	OFF	2004/12/27 11:02
S49	0	S47 same load	USPAT	OR	OFF	2004/12/27 10:59
S48	4	S47 same verilog	USPAT	OR	OFF	2004/12/27 10:59
S46	1377	simulate\$ with wire	USPAT	OR	OFF	2004/12/27 10:58
S45	3184	simulate\$ same wire	USPAT	OR	OFF	2004/12/27 10:58
S44	1	"5584598".PN.	USPAT	OR	OFF	2004/12/27 10:58
S43	1	"4496955".PN.	USPAT	OR	OFF	2004/12/27 10:57
S42	1	"5999734".PN.	USPAT	OR	OFF	2004/12/27 10:56
S41	52	half adj duplex adj. modem	USPAT	OR	OFF	2004/12/27 10:55
S30	1	NN9012277	DERVENT; IBM_TDB	OR	OFF	2004/12/27 10:32
S29	10	S28 with path	USPAT	OR	OFF	2004/12/23 16:43
S28	315	(interconnect adj2 model\$)	USPAT	OR	OFF	2004/12/23 16:42
S27	4	(interconnect adj2 model\$) same load same delay	USPAT	OR	OFF	2004/12/23 16:42
S26	66	verilog and tran	USPAT	OR	OFF	2004/12/23 13:53
S19	9	("5610833" "5629860" "5694344" "5706206" "6175947" "6189131" "6243653" "6291254" "6381730").PN.	US-PCPUB; USPAT; USOCR	OR	OFF	2004/12/23 13:50
S24	1	annotate with path with delay	USPAT	OR	OFF	2004/12/23 13:46
S23	32	wire adj. load adj. model	USPAT	OR	OFF	2004/12/23 13:46

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S22	11	S21 same simulate\$	USPAT	OR	OFF	2004/12/23 13:43
S21	129	wire adj. model	USPAT	OR	OFF	2004/12/23 13:42
S20	1	((wire or path or line) adj. (load or delay) adj. (simulate\$ or emulate\$ or model)) same verilog	USPAT	OR	OFF	2004/12/23 13:42
S15	57	model with wire with delay	USPAT	OR	OFF	2004/12/23 13:37
S18	1	(US-6763503-\$).did.	USPAT	OR	OFF	2004/12/23 11:30
S17	4	(model with wire).it.	USPAT	OR	OFF	2004/12/23 11:28
S16	0	characterize with wire with delay	USPAT	OR	OFF	2004/12/23 11:25
S14	27	timing with annotation with wire	USPAT	OR	OFF	2004/12/23 10:38
S1	177034	(simulate\$ or emulate\$)	USPAT	OR	OFF	2004/12/23 10:26
S12	32	S11 with timing	USPAT	OR	OFF	2004/12/22 17:02
S11	2968	wire with model	USPAT	OR	OFF	2004/12/22 17:00
S10	0	wire with timing with I/O with model	USPAT	OR	OFF	2004/12/22 17:00
S4	107	S3 same (port or node) same (path or loop or mesh)	USPAT	OR	OFF	2004/12/22 16:59
S9	2	(US-5428750-\$ or US-5300835-\$). did.	USPAT	OR	OFF	2004/12/22 16:58
S8	21	("4483354" "4683384" "4744084" "4791357" "4821173" "4942317" "4978633" "4980889" "5105373" "5166937" "5300835" "5317698" "5406147" "5426591" "5426739" "5428750" "5452229" "5479123" "5481484" "5535223" "5572437").PN.	US-PCPUB; USPAT; USOCR	OR	OFF	2004/12/22 16:51
S7	1	("6480817").PN.	USPAT	OR	OFF	2004/12/22 16:50
S6	5	S3 same (Verilog and VHDL)	USPAT	OR	OFF	2004/12/22 16:04
S5	5	S4 same (control\$ or detect\$ or compare\$) same (change or value)	USPAT	OR	OFF	2004/12/22 15:57
S3	14702	S1 with S2	USPAT	OR	OFF	2004/12/22 15:55
S2	2293911	(bidirection\$ or (two adj2 way) or inout or duplex) near\$3 (wire or line)	USPAT	OR	OFF	2004/12/22 15:54

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1 Space-time characteristics of ALOHA protocols in high-speed bidirectional bus networks

Whay Chiou Lee, Pierre A. Humblet
October 1995 *IEEE/ACM Transactions on Networking (TON)*, Volume 3 Issue 5

Full text available: [pdf\(14.40 KB\)](#) Additional Information: full citation, references, citations, index terms

2 Aquarius: Logic simulation on an Engineering Workstation

Andrew Sangster, Jhon Monahan
June 1983 *Proceedings of the 20th conference on Design automation*

Full text available: [pdf\(66.71 KB\)](#) Additional Information: full citation, abstract, references, citations, index terms

Aquarius is an interactive hierarchical logic simulator designed to run in a multiple window (concurrent processing) environment on an Engineering Workstation. This approach lets an engineer iterate conveniently between simulation and modification of the logic model or input patterns. Because Aquarius is hierarchical, any sub-tree of the model may be simulated, facilitating bottom-up design verification. Aquarius uses an event-driven selective trace algorithm and 9 logic states. 1 ...

Keywords: Computer-aided engineering, Engineering workstation, Interactive simulation, Logic simulation, MOS simulation

3 An adversarial model for distributed dynamic load balancing

S. Muthukrishnan, Rajmohan Rajaraman
June 1998 *Proceedings of the tenth annual ACM symposium on Parallel algorithms and architectures*

Full text available: [pdf\(181.89 KB\)](#) Additional Information: full citation, references, citations, index terms

4 Fixed-alternate routing and wavelength conversion in wavelength-routed optical networks

Ramu Ramamurthy, Biswanath Mukherjee
June 2002 *IEEE/ACM Transactions on Networking (TON)*, Volume 10 Issue 3

<http://portal.acm.org/results.cfm?coll=ACM&dl=ACM&CFID=50944889&CFTOKEN=3...> 7/26/2005

Full text available: [pdf\(461.95 KB\)](#) Additional Information: full citation, abstract, references, index terms

Consider an optical network which employs wavelength-routing crossconnects that enable the establishment of wavelength-division-multiplexed (WDM) connections between node pairs. In such a network, when there is no wavelength conversion, a connection is constrained to be on the same wavelength channel along its route. Alternate routing can improve the blocking performance of such a network by providing multiple possible paths between node pairs. Wavelength conversion can also improve the blocking ...

Keywords: WDM, adaptive routing, alternate routing, lightpath, optical network, wavelength conversion, wavelength routing

5 A performance model of deflection routing in multibuffer networks with nonuniform traffic

Joseph Bannister, Flaminio Borgonovo, Luigi Fratta, Mario Gerla
October 1995 *IEEE/ACM Transactions on Networking (TON)*, Volume 3 Issue 5

Full text available: [pdf\(1.29 MB\)](#) Additional Information: full citation, references, index terms

6 An MOS digital network model on a modified theyeven equivalent for logic simulation

Tsuyoshi Takahashi, Satoshi Kojima, Osamu Yamashiro, Kazuhiko Eguchi, Hideki Fukuda
June 1984 *Proceedings of the 21st conference on Design automation*

Full text available: [pdf\(387.72 KB\)](#) Additional Information: full citation, abstract, references, index terms

A novel analytical model of MOS digital networks, which is based on a modified Theyeven equivalent, is described. The model can handle all the primary circuits inherent in MOS technology, such as transistor logics, wired-ORs, tri-state circuits, charge-share operation, and bidirectional pass transistors etc., with precise estimation of delay time. The model has been implemented in a logic/fault simulator, named HASL-GT. Performance of 4 to 10 k events/sec has been obtained on HIT ...

7 Conservative simulation of load-balanced routing in a large ATM network model

C. D. Phan, H. Brunst, S. Fildes
July 1998 *ACM SIGSIM Simulation Digest, Proceedings of the twelfth workshop on Parallel and distributed simulation*, Volume 28 Issue 1

Full text available: [pdf\(938.77 KB\)](#) Additional Information: full citation, references, citations, index terms



8 DAB: interactive haptic painting with 3D virtual brushes

Bill Baxter, Vincent Schreib, Ming C. Lin, Dinesh Manocha
August 2001 *Proceedings of the 28th annual conference on Computer graphics and interactive techniques*

Full text available: [pdf\(10.82 MB\)](#) Additional Information: full citation, abstract, references, citations, index terms

We present a novel painting system with an intuitive haptic interface, which serves as an expressive vehicle for interactively creating painterly works. We introduce a deformable, 3D brush model, which gives the user natural control of complex brush strokes. The force feedback enhances the sense of realism and provides tactile cues that enable the user to better manipulate the paint brush. We have also developed a bidirectional, two-layer paint model that, combined with a palette interface ...

<http://portal.acm.org/results.cfm?coll=ACM&dl=ACM&CFID=50944889&CFTOKEN=3...> 7/26/2005

Keywords: Human Computer Interaction, deformable brush model, haptics, painting systems

9 AutoMod II (tutorial session)

Van B. Norman

December 1990 **Proceedings of the 22nd conference on Winter simulation**

Full text available: [pdf\(587.68 KB\)](#) Additional Information: full citation, abstract, references, citations, index, terms

10 Interactive immersion in 3D graphics: Physically based virtual painting

Ming Lin, William Baxter, Vincent Scheib, Jeremy Wendt

August 2004 **Communications of the ACM**, Volume 47 Issue 8

Full text available: [pdf\(280.71 KB\)](#) Additional Information: full citation, abstract, references, index, terms
[html\(28.71 KB\)](#)

Tapping the compelling illusion of physical interaction with paints, brushes, surfaces, color, and light, users express the nuances of their visual and emotional imaginations.

11 An adaptive, non-uniform cache structure for wire-delay dominated on-chip caches

Changyu Kim, Doug Burger, Stephen W. Keckler

October 2002 **Proceedings of the 10th international conference on Architectural support for programming languages and operating systems**, Volume 37, 30, 36 Issue 10, 5, 5

Full text available: [pdf\(1.33 MB\)](#) Additional Information: full citation, abstract, references, citations, terms

Growing wire delays will force substantive changes in the designs of large caches. Traditional cache architectures assume that each level in the cache hierarchy has a single, uniform access time. Increases in on-chip communication delays will make the hit time of large on-chip caches a function of a line's physical location within the cache. Consequently, cache access times will become a continuum of latencies rather than a single discrete latency. This non-uniformity can be exploited to provide ...

12 The second generation molis mixed-mode simulator

C. F. Chen, C-Y Lo, H. N. Nham, Prasad Subramaniam

June 1984 **Proceedings of the 21st conference on Design automation**

Full text available: [pdf\(681.47 KB\)](#) Additional Information: full citation, abstract, references, citations, index, terms

This paper describes the second generation MOTIS mixed-mode simulator. In particular, it extends the current modeling capabilities to include resistors, floating capacitors, and bidirectional transmission gates. It employs a relaxation algorithm with local time-step control for timing simulation, and a switch level approach for unit delay simulation. It provides logic and timing verification for general MOS circuits in a mixed-mode environment. The new simulator is being used for pro ...

13 On the stability of shuffle-exchange and bidirectional shuffle-exchange deflection networks

Soung C. Lew

February 1997 **IEEE/ACM Transactions on Networking (TON)**, Volume 5 Issue 1

Full text available: [pdf\(289.70 KB\)](#) Additional Information: full citation, references, index, terms

Keywords: deflection routing, hot-potato routing, network congestion, network stability, networks

packet switching, shuffle-exchange network

14 Peer to peer networks: Query-flood DoS attacks in gnutella

Neil Daswani, Hector Garcia-Molina

November 2002 **Proceedings of the 9th ACM conference on Computer and communications security**

Full text available: [pdf\(465.15 KB\)](#) Additional Information: full citation, abstract, references, citations, index, terms

We describe a simple but effective traffic model that can be used to understand the effects of denial-of-service (DoS) attacks based on query floods in Gnutella networks. We run simulations based on the model to analyze how different choices of network topology and application level load balancing policies can minimize the effect of these types of DoS attacks. In addition, we also study how damage caused by query floods is distributed throughout the network, and how application-level policies ca ...

Keywords: denial-of-service, peer-to-peer, security

15 The nesC language: A holistic approach to networked embedded systems

David Gay, Philip Lewis, Robert von Behren, Matt Welsh, Eric Brewer, David Culler

May 2003 **ACM SIGPLAN Notices, Proceedings of the ACM SIGPLAN 2003 conference on Programming language design and implementation**, Volume 38 Issue 5

Full text available: [pdf\(177.98 KB\)](#) Additional Information: full citation, abstract, references, citations, index, terms

We present nesC, a programming language for networked embedded systems that represent a new design space for application developers. An example of a networked embedded system is a sensor network, which consists of (potentially) thousands of tiny, low-power "nodes," each of which execute concurrent, reactive programs that must operate with severe memory and power constraints. nesC's contribution is to support the special needs of this domain by exposing a programming model that incorporates ...

Keywords: C, TinyOS, components, concurrency, data races, first-order, modules, nesC, programming languages

16 Load balancing, selection sorting on the hypercube

C. G. Plaxton

March 1989 **Proceedings of the first annual ACM symposium on Parallel algorithms and architectures**

Full text available: [pdf\(1.16 MB\)](#) Additional Information: full citation, citations, index, terms

17 Data file management in shift-register memories

Werner E. Kluge

June 1978 **ACM Transactions on Database Systems (TODS)**, Volume 3 Issue 2

Full text available: [pdf\(1.22 MB\)](#) Additional Information: full citation, abstract, references, index, terms

The paper proposes a shift-register memory, structured as a two-dimensional array of uniform shift-register loops which are linked by flow-steering switches, whose switch control scheme is tailored to perform with great efficiency data management operations on sequentially organized files. The memory operates in a linear input/output mode to perform record insertion, deletion, and relocation on an existing file, and in a sublinear mode for rapid internal file movement to expedite file post ...

Keywords: LIFO/FIFO operation modes, data transformations, deletion, insertion, management of sequentially organized files, record retrieval, relocation, shift-register memories, updating

18 Modeling AGV systems using network constructs

Michael W. Sale, Catherine W. Stein
December 1987 **Proceedings of the 19th conference on Winter simulation**

Full text available: [pdf\(156.22.KB\)](#)

Additional information: full citation, abstract, references, citations, index terms

The network world view of SLAM II® has been demonstrated as an effective method for modeling manufacturing processes. An automatic guided vehicle system (AGVS), however, may be difficult because of the special nature of its resources and their activities. This paper presents the Material Handling Extension for SLAM II® (MH-EX). The MH-EX overcomes these difficulties through a specialized set of network capabilities. This paper begins by describing the unique requirements I ...

19 Earthmover-simulation tool for earthwork planning

Julio C. Martinez
December 1998 **Proceedings of the 30th conference on Winter simulation**

Full text available: [pdf\(183.00.KB\)](#)

Additional information: full citation, references, citations, index terms

20 Adding a vector unit to a superscalar processor

Francisca Quintana, Jesus Corbal, Roger Espasa, Mateo Valero
May 1999 **Proceedings of the 13th international conference on Supercomputing**

Full text available: [pdf\(1.75.MB\)](#)

Additional information: full citation, references, citations, index terms

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Transmission gate modeling in an existing three-value simulator

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Proceedings of the 1980 conference on Design automation for computers
Pages 171-181
ISBN 0-89719-020-4

Author
Robert M. Madsen

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ABSTRACT

Existing three value (0, 1, X) logic simulators cannot support the use of MOS transmission gates, but this deficiency can be easily eliminated by the addition of one logic value - the high impedance (Z) state. This paper demonstrates that complete transmission gate modeling, including bi-directional operation and Ratio Logic, can be accomplished with this single Z state and explicit node models; and, since four states require the same internal storage as three states, such an enhancement would not require a major software rewrite.





REFERENCES

Note: OCR errors may be found in this Reference List extracted from the full text article. ACM has opted to expose the complete list rather than only correct and linked references.

1. P. L. Fluke, P. R. Moorby, G. Musgrave, "Logic Simulation of Bi-Directional Tri-State Gates", Proceedings of the International Conference on Circuits and Computers, Port Chester, New York, October 1-3 1980, pp. 594-600.
2. Will Sherwood, A MOS modelling technique for a state true-value hierarchical logic simulation or Karanough knowledge, Proceedings of the eighteenth design automation conference on Design automation, 6/25-28/85, June 29-July 01, 1981, Nashville, Tennessee, United States
3. J. Wantanabe, J. Miura, T. Kurachi, I. Suetsugu, "Seven Value Logic Simulation for MOS LSI Circuits", Proceedings of the International Conference on Circuits and Computers, Port Chester, New York, October 1-3, 1980, pp. 941-944.

CITINGS

P. L. Fluke, P. R. Moorby, G. Musgrave, An algebra for logic strength simulation, Proceedings of the twentieth design automation conference on Design automation, 6/6-5-6/8, June 22-29, 1983, Miami Beach, Florida, United States

- INDEX TERMS
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B.6 LOGIC DESIGN
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↑ ABSTRACT

Modelling strategies and techniques are given for static and dynamic MOS transistors in a 4-state (0/low, 1/high, Z/high-impedance, U/undefined) logic simulator environment. General MOS modelling problems are presented and a set of workable solutions are developed. Experience with these techniques is shown along with examples of MOS simulation applications. This paper discusses a technique with specific conventions for modelling MOS transistors for modelling and extending a 4-state logic simulator to include MOS modelling. The technique is meant to replace analog circuit simulation, but is aimed at increasing the accuracy of MOS logic (gate level) simulations. We begin with a general bus model and extend it to handle transistors, pullups and pulldowns, and dynamic MOS transfer gates. Extensions are shown for a bidirectional transfer gate model that can be connected in any topological configuration.

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2. Ronald E. Bryant, "MOSSIM: A Logic-Level Simulator for MOS LSI, User's Manual," Integrated Circuit Memo 80-21, MIT Department of EECS, July, 1980.
3. Carter Mead, Lynn Conway, Introduction to VLSI Systems, Addison-Wesley Longman Publishing Co., Inc., Boston, MA, 1979.
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Robert M. McDermott, Transmission gate modelling in an existing three-value simulator, Proceedings of the nineteenth design automation conference, p. 678-681, January 1992

Andrew Sangster, Jhon Monahan, Aquarius: Logic simulation on an Engineering Workstation, Proceedings of the twentieth design automation conference on Design automation, p. 93-99, June 22-29, 1983, Miami Beach, Florida, United States

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Tsuyoshi Takahashi, Satoshi Kojima, Osamu Yamashiro, Kazuhiko Eguchi, Hideki Fukuda, An MOS digital network model on a modified level-set algorithm for logic simulation, 21st Proceedings of the Design Automation Conference on Design automation, p. 253-259, June 22-27, 1984, Albuquerque, New Mexico, United States

↑ INDEX TERMS

Primary Classification:

B. Hardware

↳ B.7 INTEGRATED CIRCUITS

↳ B.7.1 Types and Design Styles

Additional Classification:

B. Hardware

↳ B.7 INTEGRATED CIRCUITS

↳ B.7.2 Design Aids

↳ Subjects: Simulation

C. Computer Systems Organization

↳ C.4 PERFORMANCE OF SYSTEMS

↳ Subjects: Modeling Techniques

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